



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,749	03/25/2004	Brian Robert Prasky	POU920030065US1	7321
33558 7590 05/26/2009 INTERNATIONAL BUSINESS MACHINES CORPORATION Richard Lau IPLAW DEPARTMENT / Bldg 008-2 2455 SOUTH ROAD - MS P386 POUGHKEEPSIE, NY 12601			EXAMINER FENNEMA, ROBERT E	
			ART UNIT 2183	PAPER NUMBER
			NOTIFICATION DATE 05/26/2009	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

poiqlaw2@us.ibm.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/809,749	<b>Applicant(s)</b> PRASKY ET AL.	
	<b>Examiner</b> ROBERT E. FENNEMA	<b>Art Unit</b> 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Claims 1-8 and 10 have been considered. Claim 1 amended as per Applicant's request.
2. Examiner notes that the current claims are inconsistent with the last entered set of claims. Notably, in Claim 1, Line 3, Applicant has added the deleted word "test" to the claim without indicating it as such. For the purposes of advancing prosecution, Examiner will not hold the case to be non-compliant, and will ignore this addition to the claim. Correction is required in the next action to make the claims consistent, and Applicant is also required to indicate if the limitation was intentionally added to the claim for this action or if it was in error.

### ***Claim Objections***

3. Claims 2-8 are objected to for referring to "A method". In order to be a proper dependent claim, they must refer to "The method", in order to further limit the method of the claim upon which they depend, and make it clear they are not referring to a different method (which would make them improper dependent claims, or independent claims themselves).
4. In Claim 1, Line 9, "the time frame of decode" lacks antecedent basis.
5. In Claim 2, Line 2, "the direction and target" lacks antecedent basis.

6. In Claim 3, Line 2, "the direction and target" lacks antecedent basis.
7. In Claim 4, Line 2, "the pipe" lacks antecedent basis.
8. In Claim 4, Line 3, "the time frame" lacks antecedent basis.
9. In Claim 5, Line 3, "the BTB" lacks antecedent basis. Applicant must either write out "branch target buffer", or indicate when the branch target buffer is first introduced that it will subsequently be referred to as BTB, such as by amending Claim 1, Line 5 to read "...and into a branch target buffer (BTB) to..."
10. In Claim 6, Line 2, "the instruction field" lacks antecedent basis. Examiner believes it is supposed to read "the instruction text field" and has interpreted it as such for the remainder of this action.
11. In Claim 6, Line 2, "the system area" lacks antecedent basis.
12. In Claim 6, Lines 3 and 4, "the BTB" lacks antecedent basis.
13. In Claim 7, Line 2, "the instruction field" lacks antecedent basis.

Art Unit: 2183

14. In Claim 7, Line 2, "the non-system area" lacks antecedent basis.

15. In Claim 10, Lines 2 and 4, "the system area" lacks antecedent basis.

16. In Claim 10, Line 3, "the BTB/BHT" lacks antecedent basis.

***Claim Rejections - 35 USC § 112***

17. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

18. Claims 1-8 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant has claimed that a Branch History Table Buffer holds an address of a branch, however, the Applicant's specification clearly states that the BHT holds predictions of taken or not taken, and that the Branch Target Buffer is responsible for holding branch addresses. One of ordinary skill in the art would not be capable of making or using a BHT which can hold an address without undue experimentation, as neither the common usage, nor definition in the specification of the BHT permits

Art Unit: 2183

allowing it to hold an address. Examiner is interpreting the claims as the specification lays out for the purposes of examination.

***Claim Rejections - 35 USC § 103***

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

20. Claims 1-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Check et al. (USPN 6,125,444, herein Check), in view of Patterson et al. (herein Patterson).

21. As per Claim 1, Check teaches: A method operating a computer having a pipelined processor (Figure 1), comprising setting a bit within an instruction text field of a branch (Column 2, Lines 33-40 and Column 4, Lines 24-27), but fails to teach:

said bit preventing the branch addresses from being placed into a branch history table and a branch target buffer to thereby prevent the branch from being written into the branch history table and branch target buffer and preventing the branch from being predicted and to make the branch only detectable as the time frame of decode.

While Check teaches using an instruction field of an instruction to disable a branch history table, he does not teach that doing so would prevent the branch from being placed in a branch target buffer, because Check is silent towards a branch target

Art Unit: 2183

buffer even existing in the system. However, Patterson teaches that in order to further increase the performance of branches, a “branch target buffer” is often used, so that the target address can be calculated in the fetch stage, instead of the decode stage (Pages 271-275). As the branch target buffer relies on having a prediction in order to determine the correct address, as seen by Figure 4.23 on Page 275, if no prediction was able to be generated, because of a BHT being disabled, then it would have been obvious to one of ordinary skill in the art to also not use the BTB, as it would not have the data it needs to be made use of, therefore, attempting to use a BTB in this situation would not only not make sense, but would be almost guaranteed to generate erroneous output. In addition, as can be seen by Column 2, Lines 28-31, sensitive system operations require cache control, so for the same reason Check disables the BHT, the BTB would need to not be written to as well. Given the advantage of a BTB as disclosed by Patterson, and the need to implement it in the system as disclosed by Check, one of ordinary skill in the art at the time the invention was made would have been motivated to include a BTB, and also to disable its use when the BHT was disabled, as the entire branch prediction mechanism must be disabled.

22. As per Claim 2, Check teaches: The method as defined in claim 1 comprising predicting the direction and target of a branch prior to decode (Figure 1).

23. As per Claim 3, Check teaches: A method as defined in claim 2 comprising predicting the direction and target of a branch prior to decode through a branch

Art Unit: 2183

prediction array (Figure 1, also see Column 4, Lines 32-49).

24. As per Claim 4, Check teaches: A method as defined in claim 1 comprising tracking the branch from the beginning of the pipe, decode, until the time frame that the given instruction is to be written into a branch prediction array (It is inherent that instructions in a pipeline are kept track of, they must exist until they are removed).

25. As per Claim 5, Check teaches: A method as defined in claim 1 comprising denoting the instruction text field as a non-writable branch into the BTB (Column 2, Lines 36-40).

26. As per Claim 6, Check teaches: The method as defined in claim 5 comprising denoting the instruction text field in the system area as a non-writable branch into the BTB in system whereby the branch is blocked from being written to the BTB (Column 2, Lines 28-31).

27. As per Claim 7, Check teaches: The method as defined in claim 6 comprising predicting the branch via aliasing (Column 4, Lines 12-15).

28. As per Claim 8, Patterson teaches: The method as defined in claim 1 wherein machine state altering code lies within an address range spanned by branch tag bits of the branch target buffer (All instructions can alter machine state, so if any instruction is



Art Unit: 2183

in the BTB, machine state altering code lies within an address range spanning by tag bits in the BTB).

29. As per Claim 10, Check teaches: The method as defined in claim 8 comprising denoting state altering code in the system area by a state bit within the BTB/BHT such that aliasing of branches is prevented within the system area (Column 2, Lines 28-40).

### ***Response to Arguments***

30. Examiner notes the typographical error in the last actions Office Action Summary form, which incorrectly indicated that the action was made final. The previous action, mailed on 12/24/2008, was a non-final action.

31. Regarding Applicants arguments in regard to the enablement rejection of Claims 1-8 and 10, Applicant has pointed to Paragraph 7 of the specification to show enablement. However, Examiner is not persuaded by this argument. Paragraph 7 (and the cited portion by the Applicant) does not show that the BHT is storing an address, and the Applicant's conclusion from that cited portion is in error. The BHT simply stores bits to indicate taken or not taken, the address is stored in the BTB, if the BHT stored addresses, then there would be no need for a BTB to even exist. Examiner also refers to the Applicant's Paragraph 28, which explicitly indicates that the branch addresses are stored in the BTB, and only in the BTB, and the BHT holds the state information (taken or not taken). The Applicant's own specification provides clear evidence that the

Art Unit: 2183

Applicant is in error in this regard. Additionally, should the Applicant require further explanation of what a BHT and a BTB is, a cursory Google search of "what is a branch history table" will generate several dozen results which will all verify that a BHT does not store addresses (except in special circumstances of a hybrid BHT/BTB which is clearly not the case here). The enablement rejection is maintained, as the Applicant's own specification explicitly discloses that the Applicant's arguments are erroneous.

On pages 6-7 of the remarks, the Applicant makes an argument that "the bit" as claimed, which "makes the branch only detectable at the time frame of decode", overcomes the teachings of Check and Patterson. Applicant further suggests that in Patterson, the fetch stage is equivalent to the cache access stage. However, Examiner notes the figure on Page 275 of Patterson, which shows that in the instruction fetch stage, the BTB will be accessed to see if there is an entry or not. However, under the Examiners combination of references, if the instruction bit of Check is set, the branch prediction mechanisms would be disabled, which would bypass this step. Therefore, clearly, a branch would not be detectable until the time of decode, because no check of the branch target buffer would take place, requiring a decode to determine the instruction type. Again, Applicant appears to be drawing in material from the specification that is not in the claims, which is not proper. The claims only indicate that a bit in a text field of an instruction prevent the branch from being predicted and to make the branch only detectable at the time frame of the decode, which is how the Check/Patterson combination would necessarily have to operate. Examiner also notes

Art Unit: 2183

that if there was no entry in the BTB (either the branch has never been encountered, or it was disabled and thus would not be accessed), Patterson explicitly teaches that the correct address is calculated in the execution stage, as seen in the left path of Figure 4.23. Patterson certainly does not teach away from the claimed limitation, as a reference "teaches away" when it states that something cannot be done. See *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1130 (Fed. Cir. 1994). This is not the case here. The target address can be calculated in the fetch stage, under certain conditions, but not under the circumstances of the rejection, and ordinarily it is calculated in the execution stage (where if there is a prediction, it is verified). None of this prevents Patterson from reading upon the claims.

32. Applicant has further argued on Page 8 that in light of Figure 4, and Paragraph 31 of the specification, that the Examiners assertion that one must disable both the BHT and the BTB if one of them is to be disabled is incorrect. However, Examiner does not see anything in this description that conflicts with the rejection. Paragraph 31 appears to be discussing what happens when a branch that has never been seen before occurs (it cannot be predicted because there is nothing to predict), and if the bit to disable writing it into the BTB/BHT, it is not written, otherwise, it is. Examiner does not see how this paragraph relates to the current rejection, or the claims, and again reminds the Applicant that for a limitation to overcome a rejection, it must be explicitly in the claims, and not in the specification. Applicant will have to elaborate on why Paragraph 31 allegedly overcomes the Examiners conclusion, as he does not see anything to

Art Unit: 2183

contradict it. If anything, Paragraph 31 supports the Examiners conclusion because it explicitly states that "If the branch is not a tagged MCEND then if the entry is current not in the BTB, it needs to be written...If the branch is a tagged MCEND, it is currently not in the BTB and should additional(sic) be blocked from being written". Therefore it seems to say that if the bit is set, it is not written, otherwise, it is.

33. Upon a closer review of the claims, Examiner has found several informalities with the claim language further detailed in the claim objections section.

34. The Examiner is available for a phone interview if the Applicant wishes to discuss any issues with the case, and any potential amendments to overcome any of the rejections, or to discuss the Examiners interpretation of the art. The Examiners phone number is listed below.

### ***Conclusion***

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

Art Unit: 2183

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT E. FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Friday, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/  
Supervisory Patent Examiner, Art Unit 2183

Robert E Fennema  
Examiner  
Art Unit 2183

RF

Application/Control Number: 10/809,749  
Art Unit: 2183

Page 13